AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application.

1–34. (Cancelled)

35. (Currently amended) A modulator comprising:

a transformer comprising a primary winding and a plurality of secondary windings;

a control driver for producing electrical control signals, said control driver being in electrical communication with said primary winding and being in electrical communication with a source of electrical power; and

a plurality of switches, each switch having an input terminal pair and at least one output terminal pair, said input terminal pair being in electrical communication with a respective said transformer secondary winding, and each switch having an input voltage limiting device in parallel with said input terminal pair, said input voltage limiting device providing a common defined voltage to each said switch;

wherein the plurality of switches are substantially simultaneously switched on by a time varying electrical control on-pulse and maintained in an on state for a predetermined extended length of time by ~~at least one~~ a plurality of time varying electrical control ~~on-pulse and/or pulses~~ on-pulses produced by said control driver, said on-pulse being substantially of a first polarity, and wherein the plurality of switches are substantially simultaneously switched off by a time varying electrical control off-pulse and maintained in an off state for a predetermined extended length of time by ~~at least one~~ a plurality of time varying electrical control ~~off-pulse and/or pulses~~ off-pulses produced by said control driver

circuit, said off-pulse being substantially of a second polarity, said second polarity being opposite to said first polarity.

36. (Previously presented) The modulator of claim 35 wherein the transformer further comprises a magnetic core having a relative magnetic permeability exceeding a magnitude of one.

37. (Previously presented) The modulator of claim 35 wherein the input voltage limiting device is comprised of devices selected from the group consisting of Zener devices and varistor devices.

38. (Previously presented) The modulator of claim 35 wherein at least one of the plurality of switches is comprised of devices selected from the group consisting of insulated gate bipolar transistors, avalanche-rated field effect transistors, and high voltage metal oxide field effect transistors.

39. (Previously presented) The modulator of claim 35 wherein the outputs of a plurality of switches are substantially connected in series.

40. (Previously presented) The modulator of claim 35 wherein the outputs of a plurality of switches are substantially connected in parallel.

41. (Previously presented) The modulator of claim 35 wherein the outputs of a

plurality of switches are connected in series/parallel combination.

42. (Previously presented) The modulator of claim 35 wherein the on-pulse further comprises a succession of similar time varying electrical control pulses of said first polarity.

43. (Previously presented) The modulator of claim 35 wherein the off-pulse further comprises a succession of similar time varying electrical control pulses of said second polarity.

44. (Previously presented) The modulator of claim 35, further including an output voltage limiting device bridging said output terminal pair, wherein said output voltage limiting device is comprised of devices selected from the group consisting of Zener devices and varistor devices.

45. (Previously presented) The modulator of claim 35, further including a series combination of a resistor and at least one Zener device in the electrically conductive path between said secondary winding and the input voltage limiting device.

46. (Previously presented) The modulator of claim 35, wherein the primary winding comprises a distributed primary winding.

47. (Currently amended) A modulator comprising:

a plurality of transformers comprising substantially a primary winding and a plurality of secondary windings;

a plurality of retriggerable drive circuits each having a buffer input terminal pair and a buffer output terminal pair, the buffer input terminal pair of each of the retriggerable drive circuits being in electrical communication with a respective member of the plurality of secondary windings and having at least one input voltage limiting device in parallel with the buffer input terminal pair, said input voltage limiting device providing a common defined voltage to each said retriggerable drive circuit;

a plurality of switches, each switch associated with a respective retriggerable driver circuit and having an output terminal pair and an input terminal pair, the input terminal pair of each switch being in electrical communication with a respective buffer output terminal pair of the retriggerable drive circuit; and

wherein each of the plurality of switches is substantially simultaneously switched on by at least one first electrical signal ~~and/or signals~~ applied to the primary and remains substantially on for a predetermined extended length of time by a first plurality of electrical signals applied to the primary until at least one second electrical signal ~~and/or signals~~ is applied to the primary ~~to maintain said plurality of switches~~ and is maintained in substantially in an off state for a predetermined extended length of time by a second plurality of electrical signals applied to the primary.

48. (Previously presented) The modulator of claim 47 wherein the transformer further comprises a magnetic core having a relative magnetic permeability exceeding a magnitude of one.

49. (Previously presented) The modulator of claim 47 wherein the voltage limiting device is comprised of devices selected from the group consisting of Zener devices and varistor devices.

50. (Previously presented) The modulator of claim 47 wherein at least one of the plurality of switches is comprised of devices selected from the group consisting of insulated gate bipolar transistors and avalanche-rated field effect transistors.

51. (Previously presented) The modulator of claim 47 wherein the outputs of a plurality of switches are substantially connected in series.

52. (Previously presented) The modulator of claim 47 wherein the outputs of a plurality of switches are substantially connected in parallel.

53. (Previously presented) The modulator of claim 47 wherein the outputs of a plurality of switches are connected in series/parallel combination.

54. (Previously presented) The modulator of claim 47 wherein at least one of the plurality of retriggerable drive circuits comprises a Zener device connected in series with a field effect transistor.

55. (Previously presented) The modulator of claim 47 wherein at least one of the

plurality of retriggerable drive circuits comprises a bipolar voltage limiting device, wherein said bipolar voltage limiting device is comprised of devices selected from the group consisting of Zener devices and varistor devices.

56. (Previously presented) The modulator of claim 47 wherein said first signal and said second signal are substantially different.

57. (Previously presented) The modulator of claim 47, further including an output voltage limiting device in parallel with said output terminal pair of at least one switch, wherein said output voltage limiting device is comprised of devices selected from the group consisting of Zener devices and varistor devices.

58. (Previously presented) The modulator of claim 47 wherein the modulator comprises a stack of modulators sharing the primary of the transformer.

59. (Previously presented) The modulator of claim 47 wherein each secondary winding of the transformer controls a respective plurality of switches.

60. (Currently amended) A modulator comprising:

a plurality of stacked transformers sharing the same primary, wherein the primary comprises at least one winding and each transformer further comprises a plurality of secondary windings; and

a plurality of switches, each switch associated with a respective

secondary winding and having input and output terminal pairs, the input terminal pair of each switch being in electrical communication with a respective secondary winding and having at least one voltage limiter in parallel with said input terminal pair, said voltage limiter providing common defined voltage to each said switch, wherein the plurality of switches are substantially simultaneously switched on by a first input signal applied to the primary and maintained in an on state for a predetermined extended length of time by a first plurality of input signals applied to the primary and switched off by a second input signal and maintained in an off state for a predetermined extended length of time by ~~at least one~~ a second plurality of input ~~signal and/or~~ signals applied to the primary.